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ABSTRACT

Self-heating effects in Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) can adversely impact both device reliability and electrical performance. Despite this, a holistic understanding of the relationship among heat transport mechanisms, device reliability, and degradation of electrical performance has yet to be established. This Letter presents an in-depth analysis of self-heating effects in GaN HEMTs using technology computer-aided design and phonon Monte Carlo simulations. We examine the differential behaviors of the maximum channel temperature (T_{max}) and the equivalent channel temperature (T_{eq}) in response to non-Fourier heat spreading processes, highlighting their respective dependencies on bias conditions and phonon ballistic effects. Our study reveals that T_{max}, a crucial metric for device reliability, is highly sensitive to both heat source-related and cross-plane ballistic effects, especially in the saturation regime. In contrast, T_{eq}, which correlates with drain current degradation, shows minimal bias dependence and is predominantly influenced by the cross-plane ballistic effect. These findings emphasize the importance of optimizing device designs to mitigate both T_{max} and T_{eq}, with a particular focus on thermal designs influenced by the heat source size. This work contributes to a deeper understanding of self-heating phenomena in GaN HEMTs and provides valuable insights for enhancing device performance and reliability.

Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) have emerged as prominent components in high-frequency and high-power applications due to their exceptional electronic properties.[1] Despite these advantages, a significant challenge associated with GaN HEMTs is device overheating.[2] This overheating threatens both the reliability and electrical performance of these devices, leading to increased focus on near-junction thermal management and electro-thermal co-design,[3,4] whereas current thermal analysis practices often rely on the maximum channel temperature (T_{max}) as the primary metric for estimating device thermal performance.[5–7] However, recent studies have demonstrated that T_{max} may not directly correlate with the electrical performance degradation in GaN HEMTs.[8,9] Instead, Chen *et al.* propose the concept of an equivalent channel temperature (T_{eq}) to better quantify such degradation.[8]

Nevertheless, these works use Fourier's law of heat conduction as the basis, which does not capture the complexity of thermal transport processes in GaN HEMTs.[8,9] Given that the dimensions of the heat source and the GaN layer in these devices are comparable to the mean free paths (MFPs) of phonons, which are the primary heat carriers in semiconductors, Fourier's law becomes inapplicable.[10,11] In such scenarios, the non-Fourier effects significantly affect the temperature field within the device and lead to elevated channel temperatures.[12–15] Our previous work has quantitatively demonstrated the influence of bias-dependent heat generation and phonon ballistic transport on the temperature distribution in GaN HEMTs.[16] We have proposed a two-thermal-conductivity model[16] to characterize the bias-dependent T_{max} based on the two-heat-source model.[17] However, the impact of phonon ballistic transport-induced temperature fields on device drain current degradation has not been thoroughly investigated. Therefore, a more comprehensive electrothermal examination that considers electrical transport and phonon thermal transport simultaneously is crucial for accurately evaluating both (T_{max}) and (T_{eq}), and for developing effective thermal management strategies to enhance device reliability and mitigate electrical performance degradation.

In this study, we employ electrothermal technology computer-aided design (TCAD) simulations, combined with phonon Monte Carlo (MC) simulations, to investigate self-heating effects in GaN HEMTs. Our analysis delves into the bias-dependent heat generation and phonon ballistic transport, examining their impacts on both the T_{max} and T_{eq}. Furthermore, we elucidate the mechanisms underlying

these impacts and explain the intricate interplay between non-Fourier heat spreading, device reliability, and the degradation of drain current due to self-heating. This work aims to deepen the understanding of self-heating phenomena and enhance near-junction thermal management strategies in GaN HEMTs.

The HEMT structure examined is illustrated in Fig. 1(a), based on the design detailed in Ref. 18. The device comprises five layers, arranged from top to bottom as follows: a SiN passivation layer, an $Al_xGa_{1-x}N$ barrier layer (with $x = 0.25$ and donor concentration $N_d = 2 \times 10^{18}$ cm^{-3}), an unintentionally doped (UID) AlGaN spacer layer ($N_d = 1 \times 10^{15}$ cm^3), a GaN buffer layer, and a SiC substrate that functions as a thermal contact. The respective thicknesses of these layers are 50 nm, 18 nm, 2 nm, 1 μm, and 10 nm. The gate length (L_g) of the HEMT is 100 nm, with source and drain access regions each extending 0.95 μm ($L_{sg} = L_{gd}$). The device modeling and simulation are carried out using Sentaurus TCAD. The Fourier's law-based thermal equation is solved to account for self-heating effects in TCAD simulations. The thermal boundary conditions include a substrate temperature fixed at 300 K, a thermal boundary resistance of 1×10^{-8} m^2 K/W, and periodic side boundaries. Various heat generation mechanisms are considered, including Joule heat, recombination heat, Thompson heat, and Peltier heat. Electron transport employs the classic drift-diffusion model (DDM), as velocity overshoot is minimally impactful in short gate length GaN HEMTs at modest drain biases,[19] with small discrepancy in heat source distributions compared to predictions by electron Monte Carlo methods.[20] Nonetheless, future work should comprehensively investigate non-local electron transport's effect on heat generation across diverse geometries and biases. The Masetti model is adopted to account for doping dependence of electron mobility,[21] and the Canali model is used to cover temperature and electric field dependence.[22] Figure 1(b) presents the simulated output characteristics of the HEMT. In the current simulation, the GaN layer adopts a thickness-dependent thermal conductivity, set at 120 W/m K. This simulation setup, particularly the model incorporating self-heating effects, demonstrates good agreement with the experimental DC results reported in Ref. 18.

To elucidate the impact of phonon ballistic effects on temperature distribution, we integrate the heat generation profiles obtained from TCAD simulations with phonon Monte Carlo (MC) simulations and finite element method (FEM) analyses.[16,23,24] The specifics of these simulations and the phonon properties utilized are detailed in Ref. 16. Figure 2 depicts the channel temperature profiles as forecasted by MC simulations and FEM under various biases while maintaining a

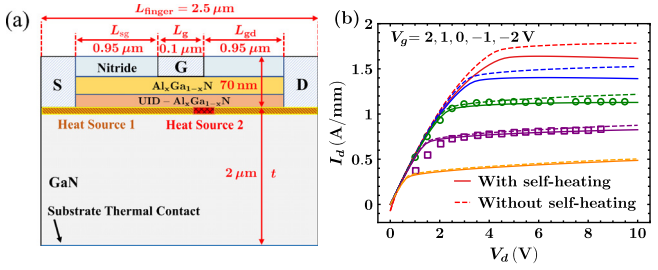

FIG. 1. (a) Schematic of the GaN HEMT. (b) Output characteristics of the HEMT extracted from TCAD simulations with GaN film thermal conductivity of 120 W/m K (lines) and experimental results (symbols).[18]

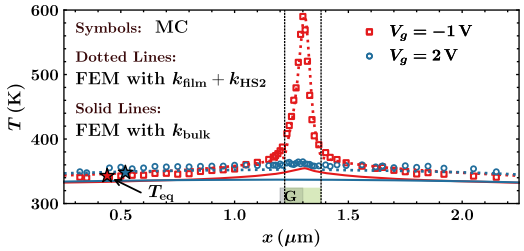

FIG. 2. Channel temperature profiles predicted by MC simulations (symbols), and FEM with k_{bulk} and $k_{film} + k_{HS2}$ at different biases with $P_{diss} = 5$ W/mm. The biasing points are $(V_g, V_d) = (-1\text{ V}, 6.7\text{ V})$ and (2 V, 3.8 V). The positions of the gate and the high-field region are marked in the figure.

consistent power dissipation ($P_{diss} = 5$ W/mm). Notably, MC simulations consistently predict higher temperatures across the channel compared to FEM using bulk thermal conductivity (k_{bulk}). This discrepancy is primarily due to two kinds of phonon ballistic effects. The cross-plane ballistic effect, stemming from phonon-boundary scattering, is influenced by the GaN layer's thickness and tends to uniformly raise channel temperatures.[25,26] In contrast, the ballistic effect with the heat source size comparable to MFP primarily elevates the temperature at the heat source.[12,16] Chen *et al.* observed that under linear operating conditions (drain-to-source voltage V_d less than saturation voltage V_{dsat}), heat dissipates uniformly across the transistor's finger (Heat Source 1, HS1).[17] However, for $V_d > V_{dsat}$, while HS1's heat dissipation peaks, additional heat generation occurs at the drain-side gate edge, forming a narrower Heat Source 2 (HS2) region.[16,17] They empirically approximated HS2 to be centered at the drain-side gate edge with a fixed length of $L_{HS2} = 160$ nm, and the approximation has been validated to be nearly independent of device geometries and biases.[17]

Although solving the phonon Boltzmann transport equation (BTE) and electron transport equations self-consistently offers the most accurate depiction of electron–phonon interactions, this approach is often too time-consuming for extensive quantitative analyses due to its high computational demands.[23] As a compromise for rapid electrothermal co-analysis, we introduce two effective thermal conductivities. The cross-plane effective thermal conductivity (k_{film}, set at 120 W/m K) accounts for the cross-plane ballistic effect. Meanwhile, a reduced thermal conductivity ($k_{HS2} = 8$ W/m K) is assigned to the HS2 region to reflect the impact of the heat source-induced ballistic effect. As shown in Fig. 2, FEM predictions using k_{film} and k_{HS2} closely align with MC simulation results across different biases. It is noteworthy that the high-field region's width remains relatively constant across varying bias conditions and device geometries, indicating that the current settings are robust for different scenarios.[16,17] By utilizing these effective thermal conductivities within TCAD simulations to ensure that the resulting temperature distributions are consistent with the MC-predicted profiles, we can investigate the interaction between thermal metrics, the bias dependence of heat generation, and the influence of phonon ballistic transport.

Figure 2 presents T_{max} and identifies the locations corresponding to the equivalent temperature T_{eq} under various bias conditions. T_{eq} is defined as the uniform temperature ($T_{uniform}$) at which a device is immersed and exhibits a drain current matching that under simulated self-heating conditions, as described by the following equation:[8]

$$T_{eq}(V_g, V_d) = T_{uniform}(V_g, V_d)|_{@I_{d,self-heating}=I_{d,uniform}}. \quad (1)$$

Interestingly, the values and positions of T_{eq} are nearly consistent across different scenarios, typically situated away from the hotspot region. This indicates that while phonon ballistic transport induced by the heat source markedly increases T_{max}, its influence on the device's electrical performance is relatively limited.

To investigate the relationship between bias dependence, phonon ballistic effects, and the temperature metrics, we perform three parallel TCAD simulations using k_{bulk}, k_{film}, and a combination of $k_{film} + k_{HS2}$. Figure 3 shows the variations in T_{max} and T_{eq} against P_{diss} for gate voltages of −1 and 2 V, under different thermal conductivity scenarios. In Fig. 3(a), T_{max} demonstrates strong bias dependency, with each curve distinctly dividing into linear and saturation regimes at V_{dsat}. Notably, at $P_{diss} = 7.5$ W/mm, even with k_{bulk}, the temperature difference between −1 and 2 V gate biases approaches 50 K. Substituting k_{bulk} with k_{film} to include cross-plane ballistic effects consistently elevates T_{max} across both regimes. Additionally, incorporating k_{HS2} leads to a slight increase in the linear regime compared to using k_{film} alone. However, beyond $V_d > V_{dsat}$, both T_{max} and its bias dependence significantly increase due to the heat source-related ballistic effect, widening the discrepancy to approximately 100 K. In contrast, Fig. 3(b) indicates that T_{eq} remains substantially lower than T_{max} for equivalent P_{diss} and shows minimal bias dependence. The T_{eq} results for scenarios with k_{film} and $k_{film} + k_{HS2}$ are closely aligned and higher than those using k_{bulk} alone. This suggests that the self-heating-induced electrical performance degradation in devices is primarily influenced by the cross-plane ballistic effect. The localized high temperatures at the drain-side gate edge, resulting from concentrated heat generation and quasi-ballistic phonon transport, have a minor impact on the degradation of the device's drain current.

Figures 4(a)–4(d) demonstrate the TCAD-predicted distributions of lateral electric field, temperature, electron mobility, and electron velocity in the channel for varying thermal conductivity settings, elucidating the distinct behaviors of T_{max} and T_{eq}. While the electric field distributions are consistent across all scenarios, employing k_{film}, a common choice in device thermal simulations, results in a uniform temperature increase across the channel compared to using k_{bulk}. Consequently, electron mobility and velocity in the access regions are adversely affected by the heightened temperatures. In scenarios incorporating $k_{film} + k_{HS2}$, the temperature in the HS2 region is specifically elevated due to the heat source-related ballistic effect, while temperatures in other channel regions mirror those observed with k_{film} alone. Despite these temperature variances in the HS2 region, the distributions of electron mobility and velocity within the channel are nearly

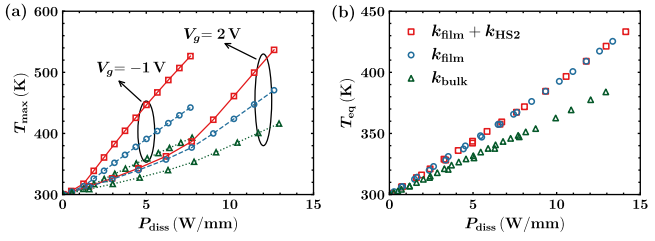

FIG. 3. (a) T_{max} and (b) T_{eq} varying with P_{diss} under two biases for various thermal conductivity settings.

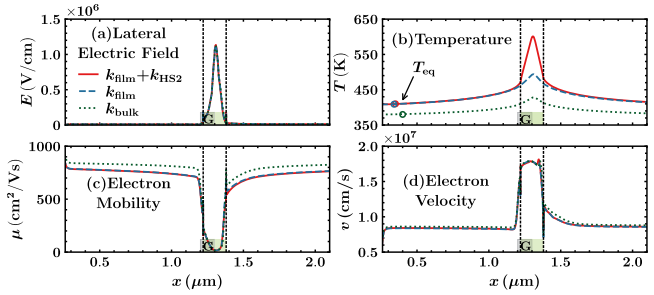

FIG. 4. Distributions of (a) lateral electric field, (b) temperature, (c) electron mobility, and (d) electron velocity along the HEMT channel with different thermal conductivity settings at $V_g = 0$Vand $V_d = 10$ V.

unchanged. This stability is attributed to the concurrent influence of electric field and temperature on these parameters. At lower fields, phonon scattering dominates electron mobility, leading to a noticeable decline as temperature increases. Conversely, at high fields, the electron velocity reaches its saturation value (v_{sat}), which is only weakly temperature-dependent.[8] In the HS2 region, the electric field is sufficiently strong that electron velocity saturates, rendering it almost impervious to temperature fluctuations. Moreover, the impact of the heat source-related ballistic effect is primarily confined to the HS2 region and does not significantly influence areas farther from the heat source, consistent with observations in other numerical studies.[12,23,27] Thus, while quasi-ballistic transport in GaN HEMTs can markedly raise the hotspot temperature, its effect on the channel electron velocity and, consequently, drain current degradation is minimal. Accordingly, the FEM simulations utilizing only k_{film} yield I–V curves that align well with experimental results, as shown in Fig. 1.

Extended simulations for HEMTs with longer gate lengths and gate-source/gate-drain spacings further support our analysis. Figures 5(a)–5(d) display the distributions of lateral electric field, temperature, electron mobility, and electron velocity in a HEMT featuring $L_g = 1\,\mu$m, $L_{sg} = 1\,\mu$m, and $L_{gd} = 3\,\mu$m. In this long-channel design, the majority of the gated region experiences a low electric field, rendering it susceptible to temperature influences. The channel resistance in this configuration is, thus, determined by both the source access region and the low-field gate portion. Notably, Fig. 5(b) shows T_{eq} shifting further into the gated region, while the high-field region at the drain-

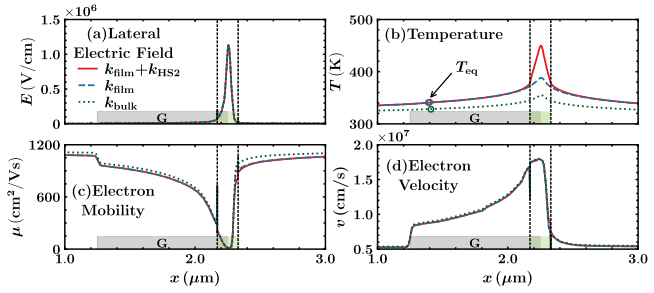

FIG. 5. Distributions of (a) lateral electric field, (b) temperature, (c) electron mobility, and (d) electron velocity along the channel of the HEMT with $L_g = 1\,\mu$m, $L_{sg} = 1\,\mu$m, and $L_{gd} = 3\,\mu$m for different thermal conductivity settings at $V_g = 0$ V and $V_d = 10$ V.

side gate edge remains unchanged in width (L_{HS2}). This indicates that even in extended-channel devices, the heat source-related ballistic transport still minimally affects the channel electron velocity.

Through the preceding analysis, the interplay between the two thermal metrics T_{max} and T_{eq}, and the non-Fourier thermal spreading process in GaN HEMTs becomes clear. T_{max}, critical for device reliability, shows strong bias-dependence and is influenced by both heat source-related and cross-plane ballistic effects. In contrast, T_{eq}, indicative of drain current degradation, exhibits minimal bias sensitivity and is primarily affected by the cross-plane effect. Optimizing device designs to mitigate these thermal metrics is crucial for enhancing reliability and reducing self-heating-induced performance degradation. In GaN HEMTs, thermal design optimization is significantly influenced by the heat source size. A small heat source can result in substantial thermal spreading resistance and concentrated heat flow at the GaN/substrate interface, emphasizing the importance of interfacial thermal resistance (TBR).[28,29] The distinct equivalent widths for T_{max} and T_{eq} necessitate careful consideration in device design to satisfy both metrics effectively.

In conclusion, this Letter presents a comprehensive analysis of self-heating effects in GaN HEMTs using TCAD and phonon MC simulations. It elucidates the distinct behaviors of T_{max} and T_{eq} in relation to non-Fourier heat spreading. T_{max} is found to be highly bias-dependent and influenced by both cross-plane and heat source-related ballistic effects, particularly in the saturation regime. Conversely, T_{eq} is less sensitive to bias and primarily impacted by the cross-plane effect. The insights gained from this study highlight the need for device designs that effectively address both T_{max} and T_{eq}, offering valuable guidance for enhancing GaN HEMT designs.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Yang Shen: Conceptualization (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Software (equal); Validation (equal); Visualization (equal); Writing – original draft (equal). **Bingyang Cao:** Funding acquisition (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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